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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/689,488	10/12/2000	Kevin Frank Smith	SJ00-00-044	7862

7590 06/03/2002

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EXAMINER
LI, ZHUO H

ART UNIT	PAPER NUMBER
2186	

DATE MAILED: 06/03/2002

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/689,488	Applicant(s) SMITH, KEVIN FRANK	
	Examiner Zhuo H Li	Art Unit 2186	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133).
- Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 October 2000* .

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-28* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14,20 and 24* is/are allowed.

6)☒ Claim(s) *1-13, 15-19, 21-23, and 25-28* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☒ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

11)☐ The proposed drawing correction filed on _____ is: a)☐ approved b)☐ disapproved by the Examiner.

If approved, corrected drawings are required in reply to this Office action.

12)☐ The oath or declaration is objected to by the Examiner.

Priority under 35 U.S.C. §§ 119 and 120

13)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____ .

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

14)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. § 119(e) (to a provisional application).

a) ☐ The translation of the foreign language provisional application has been received.

15)☐ Acknowledgment is made of a claim for domestic priority under 35 U.S.C. §§ 120 and/or 121.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449) Paper No(s) *4* .
4) ☐ Interview Summary (PTO-413) Paper No(s). _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: .

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statement filed October 12, 2000 (paper no. 4) has been considered.

Specification

2. The disclosure is objected to because of the following informalities:

Page 11 line 9, "each object 230 stores a header 230" should be --each object 230 stores a header 232-- based on figure 2.

Appropriate correction is required.

Claim Rejections - 35 USC § 112

3. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

4. Claims 1-28 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

Regarding claim 1 recites the limitation "the dynamic operation" in line 4. There is insufficient antecedent basis for this limitation in the claim.

Regarding claim 2, recites the limitation "the contents" in line 18. There is insufficient antecedent basis for this limitation in the claim.

Regarding claim 7, recites the limitation "the size", "the I/O rate", and "the hit rate" in lines 13-15. There is insufficient antecedent basis for this limitation in the claim.

Regarding claim 9, recites the limitation "the youngest member" in line 25. There is insufficient antecedent basis for this limitation in the claim.

Regarding claims 3-6, 8, and 10-19 are rejected because of depending on claim 1 respectively, containing the same deficiency.

Regarding claim 20 recites the limitation "the I/O rate" in line 10, "the hit rate" in line 11, and "the youngest member" line 21. There is insufficient antecedent basis for this limitation in the claim.

Regarding claim 21, recites the limitation "the pre-fetch scheduling module" in line 17. There is insufficient antecedent basis for this limitation in the claim.

Regarding claims 22-28 are rejected because of depending on claim 21 respectively, containing the same deficiency.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 5-6, 9-10, 15-19, 21-22 and 28 are rejected under 35 U.S.C. 102(b) as being anticipated by Yanai et al (US PAT. 5,537,568 hereinafter Yanai).

Regarding claim 1, Yanai discloses a method for scheduling prefetches into a data storage system, the method comprising remotely modeling the dynamic operation of the cache (col. 3 lines 10-17), the remotely modeling including providing a model of data elements stored within the cache (col. 4 lines 47-55) and making a cache management decision based upon the model (col. 6 lines 31-39).

Regarding claim 2, Yanai discloses to intercepting a command for a data element from a stream of Input/Output (I/O) data commands passed between a host and a storage device of the storage system (col. 4 lines 7-15) and determining whether to schedule a prefetch of a data element logically successive to the requested data element in accordance with the content of the cache as indicated by the model (col.5 lines 25-35).

Regarding claim 3, Yanai teaches that the cache is a least recently used cache (col. 6 lines 42-43).

Regarding claim 5, Yanai teaches to check the model to determine whether the requested data element is to be present with the cache (col. 4 lines 53-58).

Regarding claim 6, Yanai teaches to examine the history of a second data element stored logically adjacent to the requested data element in the storage device (col. 7 lines 57-63).

Regarding claim 9, Yanai teaches to treat a requested data element as the youngest member of the cache when the requested data element is already present in the cache (col. 8 lines 25-29).

Regarding claim 10, Yanai discloses to determine whether the data element preceding the requested data element in a sequential stream of data is also presented in the cache (col. 10 lines 30-35).

Regarding claims 15-18, Yanai teaches to periodically re-evaluate the performance of the cache model comprising the steps of determining whether the dynamic threshold used in the internal model of the cache accurately models the performance of the cache by comparing the performance of the dynamic threshold with an alternate dynamic threshold (col. 8 line 44 through col. 9 line 22).

Regarding claim 19, Yanai teaches to schedule a prefetech by sending an I/O request to the cache (col. 5 lines 15-24).

Regarding claim 21, Yanai discloses a data prefetch scheduling system comprising a cache configured to communicate with a host, and a remote prefetch module configured to communicate with the host and the cache (col. 2 lines 15-20), and configured to determine whether to schedule a prefetch of data into the cache (col. 2 lines 31-37), and a modeling module operating within the prefetch scheduling module configured to model the cache (col. 2 lines 38-45).

Regarding claim 22, the limitations of the claim are rejected as the same reasons set forth in claim 3.

Regarding claim 28, the limitations of the claim are rejected as the same reasons set forth in claim 19.

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person

having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claim 7 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yanai et al (US PAT. 5,537,568 hereinafter Yanai) in view of Kurokawa (JP 04-367954).

Regarding claim 7, Yanai teaches to determine the size of the cache and periodically fetch the I/O rate of cache (col. 5 lines 25-35). Yanai differs from the claimed invention in not specifically teaching to periodically fetch the hit rate of the cache. However, Kurokawa teaches a cache control circuit for periodically fetching the cache hit ratio in order to facilitate the development of a program whose cache-hit ratio is high. Thus, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Yanai in periodically fetching the hit rate of the cache in order to facilitate the development of a program whose cache-hit ratio is high.

9. Claim 8 is rejected under 35 U.S.C. 103(a) as being unpatentable over Yanai et al (US PAT. 5,537,568 hereinafter Yanai) in view of McNutt et al. (US PAT. 5,606,688 hereinafter McNutt).

Regarding claim 8, Yanai differs from the claimed invention in not specifically teaching to periodically calculating a single reference residency time (SRRT) for a data element within the cache. However, it is notoriously well known in the art of periodically calculating a single reference residency time (SRRT) for a data element within the cache in order to optimize the efficiency with a cache controller for maintaining useful data in the cache, for example see McNutt (abstract, col. 10 lines 52-65 and col.11 lines 41-45). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to Yanai in

periodically calculating a single reference residency time (SRRT) for a data element within the cache, as per teaching of McNutt, because it optimizes the efficiency with the cache controller for maintaining useful data in the cache.

10. Claims 11-13 and 25-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanai et al (US PAT. 5,537,568 hereinafter Yanai) in view of Dixion et al. (US PAT. 4,490,782 hereinafter Dixion).

Regarding claims 11-13, Yanai differs from the claimed invention in not specifically teaching to assign a priority value to the requested data command comprising the priority value assigned to the preceding data element plus one when the preceding data element is found to be present, and to determine whether to schedule a prefetch of a data element by comparing the priority value of the requested element with a dynamic threshold. However, Dixion teaches cache system with prefetch determined by requested record's position within data block comprising the steps of assigning a priority position to a requested data element in order to determine whether to schedule a prefetch of a data element by comparing the priority value of the requested with dynamic threshold (col. 15 line 46 through col. 18 line 59). Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Yanai in assigning the priority value to the requested data command comprising the priority value assigned to the preceding data element plus one when the preceding data element is found to be present, and to determine whether to schedule the prefetch of the data element by comparing the priority value of the requested element with a dynamic threshold, as

per teaching of Dixion, because it provides a data processor with substantially increased operating speed.

Regarding claims 25-27, the limitations of the claims are rejected as the same reasons set forth in claims 11-13.

11. Claims 4 and 23 are rejected under 35 U.S.C. 103(a) as being unpatentable over Yanai et al (US PAT. 5,537,568 hereinafter Yanai) in view of Tipley et al. (US PAT. 5,325,504 hereinafter Tipley).

Regarding claim 4, Yanai differs from the claimed invention in not specifically teaching that the LRU cache is a native cache LRU-only cache, which is not internally modified. However, it is old and notoriously well known in the art of use a native or an internal LRU-only cache because it does not account for properly reshuffling the replacement order based on read hits to a particular way, thereby increasing system efficiency. Therefore, it would have been obvious to a person of ordinary skill in the art at the time the invention was made to modify Yanai having the native LRU-only cache, as per teaching of Tipley, because it increases system efficiency so that it does not account for properly reshuffling the replacement order based on read hits to a particular way.

Regarding claim 23, the limitations of the claim are rejected as the same reasons set forth in claim 4.

Allowable Subject Matter

12. Claim 20 is allowed.

13. Claims 14 and 24 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Conclusion

14. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Shih et al. (US PAT. 5,293,609) discloses a LRU cache replacement system in which the data cache is logically partitioned into separate sections, demand and prefetch (abstract).

Tatosian et al. (US PAT. 5,490,113) discloses a memory system has a stream buffer with several performance-enhancing features. The stream buffer employs a history buffer containing the addresses of recently read memory locations in order to declare a new stream (abstract).

Tatosian et al. (US PAT. 5,461,718) discloses system for sequential read of memory stream buffer detecting page mode cycles availability fetching data into a selected FIFO, and sending data without accessing memory (abstract).

Harrison, III et al. (US PAT. 5,694,568) discloses a prefetch device is preferably integrated onto the chip and selectively issues prefetch addresses after entering an armed state induced by recognized patterns in memory operand addresses of load instructions executed by the CPU (abstract).

Miura et al. (US PAT. 5,345,560) discloses a prefetch buffer includes a buffer storage having at least one entry for storing prefetched data and an address tag, which is to be used for

searching the data, as a pair; a data searcher for searching, from the data stored in the buffer storage, for data having an address requested by the CPU (abstract).

Mayfield (US PAT. 5,664,147) discloses system and method that progressively prefetches additional lines to a distributed stream buffer as the sequentiality of the memory accessing is demonstrated (abstract).

Zangenehpour (US PAT. 5,146,578) discloses method of varying the amount of data prefetched to a cache memory in dependence on the history of data requests (abstract).

Ware et al. (US PAT. 5,537,573) discloses a cache structure and method for implementing the same takes advantage of the previous execution history of the processor and the locality of reference exhibited by the requested addresses (abstract).

15. Any response to this action should be mailed to:

Commissioner of Patents and Trademarks

Washington, D.C. 20231

Or faxed to:

(703) 308-6606

Hand-delivered responses should be brought to Crystal Park II, 2121 Crystal Drive, Arlington, VA, Fourth Floor (Receptionist).

16. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Zhuo H. Li whose telephone number is 703-305-3846. The

examiner can normally be reached on Tuesday to Friday from 9:30 a.m. to 7:00 p.m. The examiner can also be reached on alternate Monday.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Matthew Kim, can be reached on (703) 305-3821.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 305-3900.

Zhuo H. Li

Art Unit 2186

ZHL

MATTHEW KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2100